REMARKS

Applicant respectfully requests reconsideration of this application in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in substantially the same order in which the corresponding issues were raised in the Office Action.

Status of the Claims

Claims 1-21 are pending. No claims are amended. No claims are canceled. No claims are added. No new matter has been added.

Summary of the Office Action

Claims 1-21 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,512,543 to Kuroda et al. (hereinafter "Kuroda") in view of U.S. Patent No. 7,286,174 to Weale (hereinafter "Weale").

Response to Rejections under 35 U.S.C. § 103(a)

The Office Action rejected claims 1-6 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kuroda in view of Weale. Applicant respectfully requests withdrawal of these rejections because the Office Action has failed to establish a prima facie case of obviousness and the combination of cited references does not teach or suggest all of the features of the claim.

CLAIMS 1-6

Claim 1 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kuroda in view of Weale. Applicant respectfully submits that claim 1 is patentable over the combination of cited references because the combination of cited references does not teach or suggest all of the features of the claim. Claim 1 recites:

> A circuit for a pixel site in an imaging array, comprising:
> a pixel to convert incident light to an electrical signal;
> **a row line to read out a voltage from said pixel;**
> **a row line transistor, operatively connected between one end of said row line and a predetermined voltage, to reset a voltage associated with said row line;** and

a reset voltage generator, operatively connected to said row line transistor, to

generate reset pulses;

said reset voltage generator generating a first reset pulse before a beginning of an integration period of said pixel;

said reset voltage generator generating a second reset pulse after generating said first reset pulse, the generation of the second reset pulse being at an end of the integration period of said pixel. (Emphasis added).

Applicant respectfully submits that claim 1 requires a row line to read out a voltage from the pixel, a row line transistor between one end of the row line and a predetermined voltage to reset a voltage associated with said row line, and that that the reset voltage generator generates a first reset pulse before a beginning of an integration period and a second reset pulse after the first reset pulse. The cited combination fails to disclose at least these features of claim 1.

Kuroda is directed to a physical quantity distribution sensor having multiple sensor/storage sections, a selector for selecting one of the sensor/storage sections, and multiple buffers for detecting and supplying the information stored in the selected sensor/storage section. Kuroda, Abstract. More specifically, Kuroda discloses an imaging area having a pixel 32 that includes a photoelectric conversion/storage section 33, a driving transistor 35, and a pixel reset transistor 60. Kuroda, col. 6, lines 17-23. When the pixel 32 is selected, the driving transistor 35 is supplied a voltage that is substantially equal to the power supply voltage (Vdd), with no power voltage supplied to the other rows which are not selected. Kuroda, col. 6, lines 26-45. An output portion of the driving transistor 35 is connected to a corresponding load transistor through a signal line 43. The driving transistor and the load transistor 44 form a source follower circuit that produces an output, in accordance with the signal electric charge of the photoelectric conversion/storage section 33 of the pixel 32, on the signal line 43. Kuroda, col. 6, lines 48-62.

Kuroda further discloses that after the signals are read out from all the pixels in the selected row, a reset signal is applied to a selected-row-reset-driving transistor 59, which supplies a voltage to a selected pixel-reset-voltage *supply line 49*. According to the voltage on the selected line 49, a pixel reset transistors 60 in the selected row becomes electrically conductive *to clear the signal electric charges stored in the*

photoelectric conversion/storage sections 33 in the selected row. Kuroda, col. 7, lines 7-16. As seen in Figure 1, the pixel reset transistor 60 is coupled between the photoelectric conversion/storage sections 33 and the power supply line 41, and the reset signal, by way of the driving transistor 59, applies a voltage to the gate of the pixel reset transistor 60. Kuroda, Figure 1.

The Office Action purports that Kuroda allegedly discloses a row line to read out a voltage from said pixel and a row line transistor, operatively connected between one end of the row line and a predetermined voltage, to reset a voltage associated with said row line by the pixel-reset-voltage supply line 49 allegedly constituting the row line and the driving transistor 59 allegedly constituting the row line transistor. Office Action, mailed Nov. 16, 2007, page 2. Applicant respectfully disagrees with the Office Action's characterization of the cited reference.

First, Applicant respectfully submits that the pixel-reset-voltage supply line 49 is not a row line to read out a voltage from said pixel. Although Kuroda identifies row lines for the imaging area, such as nth row, (n+1) row, and (n-1) row, *these identified row lines are supply lines* that supply the power supply voltage on power supply lines 41, and the voltage from the driving transistor 59 to the selected pixel-reset-voltage *supply line* 49. As such, the supply line 49 is <u>not</u> used to *read out a voltage from said pixel, but rather to supply a voltage to the gate of the pixel reset transistor 60 to reset the voltage on the photoelectric conversion/storage section 33.* Accordingly, the pixel-reset-voltage supply line 49 does not constitute a row line to read out a voltage from said pixel, as required by claim 1.

Second, Applicant respectfully submits that the driving transistor 59 is not a row line transistor, operatively connected between one end of said row line and a predetermined voltage, because first, the driving transistor 59 is not operatively connected between one end of the row line and a predetermined voltage, and second, the driving transistor 59 does not reset a voltage associated with said row line. As described above, since the selected pixel-reset-voltage supply line 49 is not a row line to read out a voltage from said pixel, the driving transistor 59 is not operatively connected to one end of the row line. Further, although the driving transistor 59 is used in the reset process of Kuroda, the driving transistor 59 is used to reset the voltage on the photoelectric

conversion/storage section 33, not to reset a voltage associated with the row line that is for reading out a voltage from the pixel. In particular, the driving transistor 59, in response to a rest signal applied from a reset voltage input portion, supplies a voltage to the selected pixel-reset-voltage supply line 49, which is coupled to the gate of the pixel rest transistor 60, which clears the signal electric charges stored in the photoelectric conversion/storage section 33. Kuroda, col. 7, lines 7-18. As such, the driving transistor 59 does not reset a voltage associated with the row line because it merely drives a gate of another transistor that resets the charge stored in the photoelectric conversion/storage section 33, not the voltage on the row line that is read out from the pixel. Accordingly, Kuroda fails to disclose at least this feature of the claim.

It should be noted that Kuroda does disclose reading out the signals from all the pixels in the selected row. Kuroda, col. 6, line 48 to col. 7, line 8. In particular, the information stored in the photoelectric conversion/storage section 33 of the nth row is read out on the signal line 43 by supplying the supply voltage to the source follower circuits (serving as buffers), each formed by the driving transistor 35 in the nth row and the corresponding load transistor 44. Kuroda, col. 7, lines 7-16. The Applicant respectfully submits that even interpreting the signal line 43 that connects the driving transistor 35 and the load transistor 44 as the "row line to read out a voltage from said pixel," Kuroda still fails to disclose a row line transistor, operatively connected between one end of the said row line and a predetermined voltage, as discussed above.

Applicant respectfully submits that Weale fails to cure the above deficiencies of Kuroda. Accordingly, the combination of cited references does not teach or suggest all of the features of the claim. Given that the combination of the references fails to teach or suggest all of the features of claim 1, Applicant respectfully submits that claim 1 is patentable over the combination of cited references. Accordingly, Applicant requests that the rejection of claim 1 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 2-6 depend from independent claim 1, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 2-6 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 2-6 under 35 U.S.C. § 103(a) be withdrawn.

CLAIMS 7-14

Claim 7 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kuroda in view of Weale. Applicant respectfully submits that claim 7 is patentable over the combination of cited references because the combination of cited references does not teach or suggest all of the features of the claim.

Claim 7 recites:

A method for measuring a pixel voltage using a row line, comprising:
(a) hard resetting the **row line voltage** to a first predetermined voltage;
(b) soft resetting the row line voltage to a first pixel voltage;
(c) hard resetting the row line voltage to a second predetermined voltage;
(d) soft resetting the row line voltage to a second pixel voltage; and
(e) determining a difference between the first and second pixel voltages, the difference being the measured pixel voltage. (Emphasis added).

Applicant respectfully submits that claim 7 requires hard resetting **a row line voltage** twice and soft resetting the row line voltage twice. The cited combination fails to disclose at least these features of claim 7.

As described above, Kuroda is directed to resetting the charge on the photoelectric conversion/storage section 33, not resetting a row line voltage. As such, Kuroda fails to teach or suggest hard resetting the row line voltage to a first predetermined voltage, for example. Weale fails to cure the deficiencies. Accordingly, the combination of cited references fails to teach or suggest all of the features of the claim. Given that the combination of the references fails to disclose all of the features of claim 7, Applicant respectfully submits that claim 7 is patentable over the cited references. Accordingly, Applicant requests that the rejection of claim 7 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 8-14 depend from independent claim 7, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 8-14 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 8-14 under 35 U.S.C. § 103(a) be withdrawn.

CLAIMS 15-21

Claim 15 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Kuroda in view of Weale. Applicant respectfully submits that claim 15 is patentable

over the combination of cited references for similar reasons described above with respect to claims 1 and 7. In particular, neither Weale nor Kuroda discloses a row line including a row line transistor as described above with respect claim 1. Given that the combination of the references fails to disclose all of the features of claim 15, Applicant respectfully submits that claim 15 is patentable over the cited references. Accordingly, Applicant requests that the rejection of claim 15 under 35 U.S.C. § 103(a) be withdrawn.

Given that claims 16-21 depend from independent claim 15, which is patentable over the cited reference, Applicant respectfully submits that dependent claims 16-21 are also patentable over the cited reference. Accordingly, Applicant requests that the rejection of claims 16-21 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

It is respectfully submitted that in view of the remarks set forth herein, the rejections have been overcome. If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Daniel Ovanezian at (408) 720-8300.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

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